Centre tapped transformer in multisim

Highlighted Highlighted Highlighted Circuit Description Smart StudyChat Please review the following videos before starting with this lab: Materials and Equipment: Materials: Simulators (Multisim): Central 30/3 Vrms TwoDedes 1N4001 Two 2.2 kΩ A 100 µF, Electrolysis 50 V A fuse (any rating is good because it is only for simulation) Hardware parts (In toolbox): Two iodines 1N4001 Two 2.2 kΩ A 100 µF condense, 50 V Capacitor: Multisim: Agilent Function Generator Tektronix oscilloscope Hardware Equipment: Breadboard NI myDAQ Instrument Device Screw Driver Terminal connector Jumper wires Oscilloscope and Function generator from NI ELVISmx Intrument Launcher Procedure : ***** This lab must be implemented in both software (running simulations on Multisim) and hardware (using NI myDAQ) ***** Part A: Half-Wave Editing: Figure 1 Software (Multisim): Build a half-wave rectanining circuit in Figure 1 in Multisim. Use a functional generator to deliver Vacand's AC input using a extraction center variable to get VSEC. Be sure to establish the tolerance of the force to 20%. Connect the Tektronix oscillation so that channel 1 is on the transformer and channel 2 is horizontally across the load return (RL). Observe VSEC and VLOAD wave formats. The input is not very useful as a dc source because of variations in the wavelength of the input. Connect a capacitors of 100 µF (C1) with a tolerance of 20% parallel to the load capacitors (RL). (Note the polarity of capacitors). Measure the dc load voltage, VLOAD and peak ripple voltage, VRIPPLE, of the input. Measure the frequency of ripples. Tabulate all the data collected and compare the results with and without filter capacitors. Hardware (NI myDAQ): Using the VSEC voltage obtained from the simulation, build the circuit in Figure 1 on the breadboard with VSEC as input, connect to the diode and the RL load voltage in sequence. (See Figure 3) Using jumping wires, screw drivers and screw terminal connectors, connect the board to the Ni MyDAQ Instrument Device for circuit analysis. Use the AO0 channel on the myDAQ NI Instrument Device to provide input (VSEC) and AI0 channels to measure the input voltage (VLOAD). Use a functional generator from the NI ELVISmx Instrument Launcher, which provides VSEC input voltage for the circuit. Measure the VLOAD input voltage, on the load RL by oscillation. Repeat steps 3 and 4 with a capacitors of 100uF if you notice any variations in the input. Figure 2 Evaluating the question: What is the purpose of having a half-wave receding in the circuit? Description: what are the procedures in this lab to go to the final design of both hardware and software to achieve the design goals? Discuss the impact of having capacitors on the input voltage and the effect of additional loads on the ripple voltage. Deliverables: VSEC voltage measurement, top voltage of the input, VLOAD and ripple voltage VRIPPLE. Take a screenshot of your measurements from Multisim. Place your student ID card on the breadboard and take pictures of the circuit board and battery out on the myDAQ NI device. Take a screenshot of measurements obtained from the functional generator and oscillating on the ELVISmx NI tool launcher on your screen. Part B: Full Wave Editing: Software (Multisim): Build a half-wave receding circuit in Figure 3 in Multisim. Use a functional generator to deliver Vacand's AC input using a extraction center variable to get VSEC. Notice that the ground for the circuit has changed. Check your circuit carefully before applying power. Connect the Tektronix oscillation so that each channel passes through each diode. Observe the VSEC wavelengths on each diode and then observe the VLOAD. Connect a capacitors of 100 µF (C1) with a tolerance of 20% parallel to the load capacitors (RL). (Note the polarity of capacitors). Measure the dc load voltage, VLOAD and peak ripple voltage, VRIPPLE, of the input. Measure the frequency of ripples. Tabulate all the data collected and compare the results with and without filter capacitors. Figure 3 Hardware (NI myDAQ): Uses double the VSEC voltage obtained from the simulation, building the circuit in Figure 3 on the breadboard with 2* VSEC as input, connecting to two iodine and RL load return in the chain. (See Figure 4) Using jumping wires, screw drivers and screw terminal connectors, connect the board to the Ni MyDAQ Instrument Device for circuit analysis. Use the AO0 channel on the myDAQ NI Instrument Device to provide input (2* VSEC) and AI0 channels to measure the input voltage (VLOAD). Use a functional generator from the NI ELVISmx Instrument Launcher, which provides VSEC input voltage for the circuit. Measure the VLOAD input voltage, on the load RL by oscillation. Repeat steps 3 and 4 with a capacitors of 100uF if you notice any variations in the input. Figure 4 Question review: What is the purpose of having a full wave rec adjuster in the circuit? Description: what are the procedures in this lab to go to the final design of both hardware and software to achieve the design goals? Discuss the impact of having capacitors on the input voltage and the effect of additional loads on the ripple voltage. How is the full wave resymlver's input different from half-wave resythnger? Deliverables: VSEC voltage measurement, top voltage of the input, VLOAD and VRIPPLE ripple voltage. Take a screenshot of your measurements from Multisim. Place your student ID card on the breadboard and take pictures of the circuit board and battery out on the myDAQ NI device. Take screenshots of your measurements from the Ni ELVISmx Instrument Launcher showing both input from the functional generator and the above oscillating on your screen. Lab Report: Use lab report samples found in tool and sample links in Center. Includes all products transferred from Part A and Part B. Includes all screenshots of measurements from Multisim, breadboard circuit design using myDAQ NI equipment and measurements from MI ELVISmx Instrument Launcher. Save the document as Lab2YourGID.docx (e.g. Lab2G00050331.docx) and send it in the Blackboard. Grading criteria A-grade: Half-wave reclamation circuit in Multisim - with and without filter capacitor10Part A: Half-wave rectanine circuit on NI myDAQ and breadboard with and without filter capacitor10Part A: Transfer equipment: Measurement and screen capture from Multisim and hardware15Review Questions10Part B: Full wave rectanine circuit in Multisim - with and without filter capacitor10Part B : Full wave tuning circuit on NI myDAQ and breadboard with and without filter capacitor10Part B: Deliverables: Measurement and screen capture from Multisim and hardware15Review Questions10Report format (Proper use of template)10TOTAL100 ET 212 Lab Half Homework-Wave and Full-Wave RectifierPurchase the answer to view itET212LabHomework : Deliverables: Measurement and screen capture from Multisim and hardware15Review Questions10Report format (Proper use of template)10TOTAL100 ET 212 Homework Lab Half-Wave and Full-Wave RectifierPurchase the answer to view itET212LabHomework : Deliverables: Measurement and screen capture from Multisim and hardware15Review Questions10Report format (Proper use of template)10TOTAL100 ET 212 Lab Homework Half-Wave and Full-Wave RectifierPurchase the answer to view itET21Half-WaveandFull-WaveRectifier.zipET212LabHomeworkHalf-WaveAndFull-WaveRectifiernew.docxET212LabHomeworkHalf-WaveAndFull-WaveRectifierNew.zip NI does not actively maintain this material. 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